Remarks

Claims 2, 3, and 6 are objected to as being dependent upon a rejected base claim. Claims 1 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li (US 6,023,778). Claims 5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li and further in view of Srinivasan et al. (US 6,698,006).

1. Rejection of claims 1 and 4 under 35 U.S.C. 103(a):

Claims 1 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li (US 6,023,778) for reasons of record, as recited on pages 3-4 of the above-indicated Office action.

Response:

The applicant would like to point out the patentable differences between the limitations contained in claim 1 and what is taught in the Li patent.

Claim 1 of the present invention contains the limitations of a first input node for receiving raw data, a second input node for receiving test data, a selection node for selecting input from the first or second node, and a delay circuit. The delay circuit is used for delaying the test data input to the second node so that the test data and the raw data would reach an output node of the multiplexer after experiencing the same amount of delay.

It is important to note that in the present invention, it is not the selection signal that is being delayed, but rather one of the data inputs of the multiplexer. Since there are at least two data inputs used in the multiplexer, the present invention insures that the data reaches the output of the multiplexer after the same amount of delay.

The Li patent, on the other hand, does not teach delaying one of the data inputs of a multiplexer for ensuring that the data signals reaching the output of the multiplexer have experienced the same delays. Instead, Li teaches **delaying**

the selection signal that controls which of the inputs to the multiplexer is used.

In col.1, lines 24-26, Li states that a scan mode signal is used as a selection signal for selecting a system mode or a test mode. In col.1, lines 60-67, Li clearly states that the scan mode signal contains a value of one or zero for selecting the input to the mux scan flip flops.

In col.3, lines 58-59, Li teaches using a delay circuit 54 for receiving and delaying scan mode signals. The output 55 from the delay circuit 54 is used as scan mode inputs 56, 58, 71, 77, and 83 for acting as selection signals for the various mux flip-flops 62, 68, 75, 81, 87 (col.3, line 66 to col.4, line 2). Delaying the selection signal in no way affects the relative delay between raw data and test data entering the multiplexer.

Therefore, Li does not teach all of the limitations recited in claim 1 of the present invention. That is, Li does not teach "a delay circuit electrically connected **between the second input node and the output node** for prolonging a traveling time which the **test data** takes to travel from the second input node to the output node," as is required by claim 1 of the present invention.

In view of the above, claim 1 is not anticipated by Li since Li does not teach all of the limitations of claim 1. The differences between the limitations contained in claim 1 and the Li patent would also not have been obvious to one skilled in the art since the present invention treats a completely different problem that is not mentioned or contemplated by the Li patent. Since claims 2-7 are all dependent on claim 1, they should be allowed if claim 1 is allowed. Reconsideration of claims 1-7 is respectfully requested.

Respectfully submitted,

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